IN THE CLAIMS

The status of the claims as presently amended is as follows (changes highlighted):

1. (Currently Amended) A lateral semiconductor device comprising:

a semiconductor chip;

two main electrodes on one major surface of the semiconductor chip; and

an alternating conductivity type layer between the main electrodes;

wherein the alternating conductivity type layer comprises first semiconductor regions of a first conductivity type and second semiconductor regions of a second conductivity type;

wherein the first semiconductor regions and the second semiconductor regions are alternately arranged in a surface portion of the major surface;

wherein the alternating conductivity type layer comprises a closed loop formed by the first and second semiconductor regions alternately arranged along the direction of the closed loop and surrounding one of the main electrodes; and

wherein the alternating conductivity type layer comprises at least one straight ~~sections~~section and at least one curved ~~sections~~section; and

wherein the closed loop is formed in a laminated direction of the first semiconductor regions and the second semiconductor regions, and a lateral width of the first semiconductor regions and the second semiconductor regions forming the closed loop in the straight ~~sections~~section is the same.

2. (Previously Amended) A lateral semiconductor device comprising:

a semiconductor chip;

two main electrodes on one major surface of the semiconductor chip; and

an alternating conductivity type layer between the main electrodes;

wherein the alternating conductivity type layer comprises first semiconductor regions of a first conductivity type and second semiconductor regions of a second conductivity type;

wherein the first semiconductor regions and the second semiconductor regions are alternately arranged;

wherein the alternating conductivity type layer comprises a closed loop surrounding one of the main electrodes;

wherein the alternating conductivity type layer comprises first and second sections, wherein the first semiconductor regions and the second semiconductor regions are arranged alternately at a first pitch in the first section, and the first semiconductor regions and the second semiconductor regions are arranged alternately at a second pitch different from the first pitch in the second section; and

wherein the closed loop is formed in a laminated direction of the first semiconductor regions and the second semiconductor regions, and a lateral width of the first semiconductor regions and the second semiconductor regions forming the closed loop is the same.

3. (Canceled)

4. (Previously Amended) The lateral semiconductor device according to Claim 1, wherein the alternating conductivity type layer comprises at least two straight sections and at least two curved sections.

5. (Original) The lateral semiconductor device according to Claim 4, wherein the alternating conductivity type layer comprises at least four straight sections and at least four curved sections.

6. (Currently Amended) A lateral semiconductor device comprising:

a semiconductor chip;

two main electrodes on one major surface of the semiconductor chip; and

an alternating conductivity type layer between the main electrodes;

wherein the alternating conductivity type layer comprises first semiconductor regions of a first conductivity type and second semiconductor regions of a second conductivity type;

wherein the first semiconductor regions and the second semiconductor regions are alternately arranged;

wherein the alternating conductivity type layer comprises a closed loop surrounding one of the main electrodes;

wherein the alternating conductivity type layer comprises at least one straight ~~sections~~section and at least one curved ~~sections~~section;

wherein the first semiconductor regions and the second semiconductor regions are arranged alternately at a first pitch in the straight ~~sections~~section, and the first semiconductor regions and the second semiconductor regions are arranged alternately at a second pitch in the curved ~~sections~~section, the second pitch being different from the first pitch; and

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wherein the closed loop is formed in a laminated direction of the first semiconductor regions and the second semiconductor regions, and a lateral width of the first semiconductor regions and the second semiconductor regions forming the closed loop in the straight ~~sections~~section is the same.

7. (Previously Amended) The lateral semiconductor device according to Claim 6, wherein the first pitch is equal to or longer than the second pitch.

8. (Currently Amended) The lateral semiconductor device according to Claim 6, wherein the curved ~~sections are~~section is doped substantially more lightly than the straight ~~sections~~section.

9. (Currently Amended) The lateral semiconductor device according to Claim 8, wherein the curved ~~sections are~~section is substantially intrinsic.

10. (Original) The lateral semiconductor device according to Claim 8, wherein the first pitch is shorter than the second pitch.

11. (Currently Amended) The lateral semiconductor device according to Claim 8, wherein the curved ~~sections are~~section is doped with an n-type impurity and a p-type impurity.

12. (Currently Amended) The lateral semiconductor device according to Claim 9, wherein the curved ~~sections are~~section is doped with an n-type impurity and a p-type impurity.

13. (Currently Amended) The lateral semiconductor device according to Claim 6, wherein the lateral width of at least a portion of the curved ~~sections~~section is larger than the lateral width of the straight ~~sections~~section.

14. (Previously Amended) The lateral semiconductor device according to Claim 1, further comprising a plurality of closed loops, each including the alternating conductivity type layer.

15. (Original) The lateral semiconductor device according to Claim 1, wherein the width of the first semiconductor region or the second semiconductor region is from 1/4 to 4 times as large as the depth of the first semiconductor region or the second semiconductor region respectively.

16. (Original) The lateral semiconductor device according to Claim 1, wherein the width of the alternating conductivity type layer is from 12.5 to 100 times as large as the width of the first semiconductor region or the second semiconductor region.

17. (Original) The lateral semiconductor device according to Claim 16, wherein the width of the alternating conductivity type layer is from 12.5 to 100 times as large as the depth of the first semiconductor regions or the second semiconductor regions.

18-30 (Canceled)

31. (Previously Amended) The lateral semiconductor device according to Claim 1, wherein the lateral semiconductor device comprises a semiconductor device selected from the group consisting of a MOSFET, a bipolar transistor, an IGBT, and a diode; one of the two main electrodes having a, high potential is inside the closed loop, and the other of the two main

electrodes having a low potential is outside the closed loop.

32. (Previously Canceled)

33. (Currently Amended) The lateral semiconductor device according to Claim 1, further including a circuit for controlling the semiconductor device, for protecting the semiconductor device, and for detecting the states of the semiconductor device, the circuit being outside the closed loop.

34. (Canceled)